CLAIMS

What is claimed is:

1. A clock squarer having a semiconductor chip pad and a square wave generating circuit, the clock squarer including a capacitor provided between the semiconductor chip pad and the square wave generating circuit, wherein, in response to an input signal at the chip pad, a square wave having a stable duty is generated at an output of the square wave generating circuit, irrespective of variance in environmental conditions.

2. The clock squarer of claim 1 wherein the environmental conditions include at least one of temperature, process and supply voltage.

3. The clock squarer of claim 1 wherein the capacitor is provided in series between the semiconductor chip pad and the square wave generating circuit.

4. The clock squarer of claim 1, wherein the square wave generating circuit comprises:

an inverter receiving an output signal of the capacitor and inverting the signal;

a feedback resistor connected in parallel with the inverter; and

a Schmitt trigger circuit receiving an output signal of the inverter and, in response, generating a square wave.

5. The clock squarer of claim 1, wherein the capacitor comprises a Metal-Insulator-Metal (MIM) capacitor.

6. A clock squarer, comprising:

a semiconductor chip pad for connecting an external circuit with an internal circuit of a semiconductor chip;

an electrostatic protective circuit connected to the semiconductor chip pad;

a capacitor having a first terminal connected to the semiconductor chip pad; and

a square wave generating circuit connected to a second terminal of the capacitor for generating a square wave at an output terminal thereof based on an

input signal received at the semiconductor chip pad.

7. The clock squarer of claim 6, wherein the electrostatic protective circuit comprises:

a PMOS transistor diode-connected between the semiconductor chip pad and a supply voltage; and

an NMOS transistor diode-connected between the semiconductor chip pad and a ground voltage.

8. The clock squarer of claim 6, wherein the square wave generating circuit comprises:

an inverter receiving an output signal of the capacitor and inverting the signal;

a feedback resistor connected in parallel with the inverter; and

a Schmitt trigger circuit receiving an output signal of the inverter and, in response, generating a square wave.

9. The clock square of claim 6, wherein the capacitor is comprises a Metal-Insulator-Metal (MIM) capacitor.

10. The clock squarer of claim 6 wherein the capacitor is connected in series between the semiconductor chip pad and the square wave generating circuit.